What is Claimed Is:

1. A method of manufacturing a semiconductor device, the method comprising:

forming two gate electrode structures, spaced apart by gap, on a semiconductor substrate;

depositing an undoped oxide liner on the gate electrode structures and into the gaps; and

depositing a layer of boron (B) and phosphorous (P)-doped silicon oxide (BPSG) on the undoped oxide liner filling the gap.

2. The method according to claim 1, comprising depositing an undoped silicon oxide liner, as the undoped oxide liner, by sub-atmospheric-chemical vapor deposition (SA-CVD).

3. The method according to claim 2, comprising depositing the undoped silicon oxide liner at a thickness of 400Å to 600 Å.

4. The method according to claim 2, comprising the BPSG layer in-situ by SA-CVD.

5. The method according to claim 2, comprising depositing the undoped silicon oxide liner in a deposition chamber at:

a tetraethyl orthosilicate (TEOS) flow rate of 400 to 600 mgm;

an ozone (O_3) flow rate of 3,600 to 4,400 sccm;

a helium (He) flow rate of 5,400 to 6,600 sccm;

a pressure of 180 to 220 Torr;

a temperature of 460°C to 500°C; and

a spacing of 200 to 240 mils.

6. The method according to claim 5, comprising depositing the undoped silicon oxide liner at a thickness of 400Å to 600Å.

7. The method according to claim 5, comprising depositing the layer of BPSG in-situ, by introducing into the deposition chamber:

triethylborate (TEB) at a flow rate of 123 to 183 mgm; and

triethylphosophate (TEPO) at a flow rate of 31 to 71 mgm; and

continuing SA-CVD deposition at:

a TEOS flow rate of 400 to 600 mgm; and

an O_3 flow rate of 3,600 to 4,400 sccm;

a He flow rate of 5,400 to 6,600 sccm;

a pressure of 180 to 220 Torr;

a temperature of 460°C to 500°C; and

a spacing of 200 to 240 mils.

8. The method according to claim 1, where the gate electrode structures comprise:

a tunnel oxide on the semiconductor substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate on the interpoly dielectric.

9. The method according to claim 8, wherein further comprising a silicon oxide spacer on side surfaces of the gate electrode structure.

10. A semiconductor device comprising:

two gate electrode structures, spaced apart by a gap, on a semiconductor substrate;

an undoped oxide liner on the gate electrode structures in the gap; and

a layer of boron (B) and phosphorous (P)-doped silicon oxide (PBSG) on the undoped oxide liner filling the gap.

11. The semiconductor device according claim 10, wherein the undoped oxide liner has a thickness of 400Å to 600Å.

12. The semiconductor device according to claim 10, where the undoped oxide liner comprises undoped silicon oxide derived from tetraethyl orthosilicate (TEOS).

13. The semiconductor device according to claim 10, wherein the gate structures comprise:

a tunnel oxide on the semiconductor substrate;

a floating gate electrode on the tunnel oxide;

an interpoly dielectric comprising an oxide/nitride/oxide (ONO) stack on the floating gate; and

a control gate on the interpoly dielectric.

14. The semiconductor device according to claim 13, further comprising a silicon oxide spacer on side surfaces of the gate electrode structures.